RISC vs CISC: Settling a 40 Year Old Debate

Introduction

This paper seeks to answer a simple question that has been keeping computer architects up at night for the last 40 years: RISC or CISC?

First, the concepts of both RISC and CISC processors will be explained in detail. From there, academic papers comparing RISC and CISC chips against each other will be scrutinized to determine which processor is superior. Finally, some of the alternatives to RISC and CISC processors will be examined and future developments in Instruction Set Architecture (ISA) will be discussed.

What is RISC?

The term "Reduced Instruction Set Computer" or RISC was coined by David A. Patterson and David R. Ditzel in their 1980 article for *Computer Architecture News* entitled *The case for the reduced instruction set computer*.

Every computer has an instruction set (a group of machine language instructions) that helps it execute code (PCMag, n.d.). Without this instruction set, it would be impossible to run programs on the computer and thus the computer itself would become obsolete (PCMag, n.d.).

At the time of Patterson and Ditzel's article, computers had been trending towards more and more complicated instruction sets in an attempt to improve performance, achieve code density, support high level languages and sell more chips.

Patterson and Ditzel found that this increased complexity was unnecessary.

In the IBM 360 compiler, for example, only 30 instructions accounted for 99% of all instructions executed by the computer (Patterson and Ditzel, 1980). Due to this, the pair suggested reducing the number of instructions on the computer hence the idea of the "Reduced Instruction Set Computer".

One of the first RISC projects to be implemented was the MIPS processor (Chen et al., n.d.). MIPS was brainstormed during a class for graduate students at Stanford in the early 1980s and contained around 111 instructions represented in 32 bits (Chen et al., n.d.). According to Chen et al., some examples of instructions found on the processor included arithmetic instructions, logic instructions, bit manipulation instructions, comparison instructions, jump instructions, load instructions, store instructions and move instructions.

The MIPS project and all RISC processors since then have had three main characteristics (in addition to a smaller instruction set): one cycle execution time, pipelining and a large number of registers (Chen et al., n.d.).

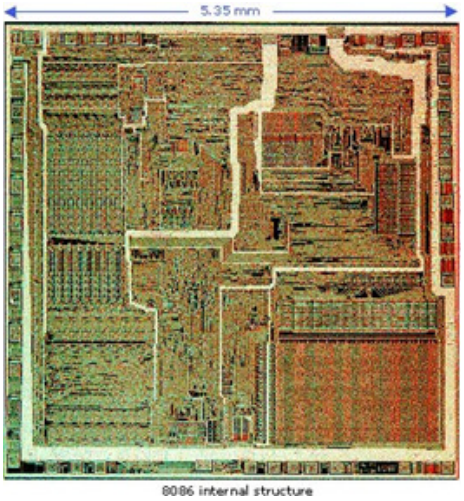
According to Chen et al., one cycle execution time means that the processor executes one instruction per cycle. Due to this, RISC processors can utilize pipelining to execute more instructions in a shorter period of time. Finally, a large number of registers are needed in RISC chips to prevent large amounts of interactions with the memory (Chen et al., n.d.).

What is CISC?

Incidentally, in the same 1980 article by Patterson and Ditzel, the term "Complex Instruction Set Computer" or CISC was coined. As opposed to RISC architecture, CISC architectures have a lot more instructions that are specialized to specific tasks (Patterson and Ditzel, 1980). The goal of this is to complete tasks in as few lines of assembly language as possible (Chen et al., n.d). According to Chen et al., an example of an instruction found in a CISC processor could be one specifically for multiplying numbers.

CISC chips are characterized by having multi-clock cycles (instructions can be executed over multiple cycles), a more efficient use of RAM than RISC chips, instructions that vary in length (meaning pipelining is a lot harder) and the use of transistors to store instructions instead of memory registers (Chen et al., n.d.).

One of the earliest CISC processors was the 1978 Intel 8086 which had around 120 instructions. According to Old-Computers.com the 8086 had only 1 Megabyte of RAM and was 16 bits. Despite this, the 8086's architecture was so good that it is still present in Intel's x86 family today (Old-Computers.com., n.d.).



The internal structure of the Intel 8086. Credit: Old-Computers.com.

RISC vs CISC

RISC vs CISC was a big debate in the 1980s and 1990s and was the topic of many scholarly articles from that time.

Douglas Barney's 1989 article, *Battle chips steaming away*, argued that RISC chips ran a lot faster than CISC chips but took more effort to create. According to Barney, the race between RISC and CISC was close but RISC is the winner because "each time CISC systems catch up, the RISC ones will again leap ahead" (Barney, p.37).

A 1993 article entitled *PC vendors warm up to RISC technology* explained that PC vendors were considering RISC chips for their next-generation servers. According to the article, analysts agreed that RISC vendors had the potential to overtake CISC.

An article from 1989 entitled *RISC vs CISC* recounts the results of a test by Jim Geers, the president of AIM Technology. In this test, Geers pitted RISC computers against CISC computers and found that RISC vastly outperformed CISC. In fact, the RISC chips doubled and tripled the performance of CISC architectures in Unix based tests (Hamilton, 1989).

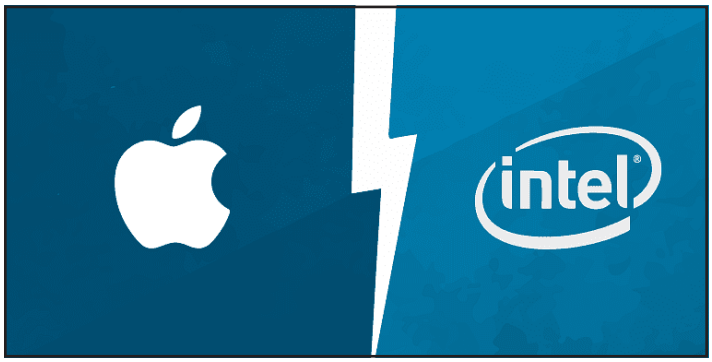
Finally, a 1995 article entitled *RISC versus CISC* by Tariq Jamil explained that RISC chips were superior because a majority of instructions on CISC chips were never used. The article then described how the (then) technology giants IBM, Motorola and Apple were trying to develop RISC chips with their PowerPC family of processors. The article concluded by saying that, while the RISC and CISC debate was far from over, some form of RISC would eventually need to be implemented in all chips.

From these articles, it is clear that RISC processors were superior to CISC processors in the 1980s and 1990s both from a theoretical and a practical standpoint.

However, like everything else in technology, things change. CISC manufacturers started copying parts of RISC chips and RISC manufacturers started copying parts of CISC chips (Chen et al., n.d.). CISC chips began implementing pipelining and RISC chips began loading more complicated instructions (Chen et al., n.d.). Soon, the RISC vs CISC debate started to become a pointless one because the technologies had become so similar.

In fact, the technologies had become so similar to each other that the term "Complex-Reduced Instruction Set Computers" or CRISC was mentioned by two researchers in a 2007 paper entitled *A New Trend for CISC and RISC Architectures*. According to the researchers, Intel's Pentium chips were so much of a hybrid between RISC and CISC they could no longer be defined as one or the other.

Today, architectures continue to be falsely labeled as RISC or CISC. ARM chips used in Apple products are commonly labelled "RISC" and Intel's x86, used in the majority of personal computers, are commonly labelled "CISC" (Hruska, 2021). However, as Joel Hruska points out in his 2021 article, ARM is not a true RISC processor as it uses out-of-order execution, SIMD execution units and branch prediction; technologies that were not invented at the time of Patterson and Ditzel. Similarly, Intel's x86 chips decode instructions into RISC style micro-operations before executing them meaning they cannot be truly classified as "CISC" (Hruska, 2021).



Apple's ARM chips are falsely labelled as RISC and Intel's x86 chips are falsely labelled as CISC. Credit: Futurm Research.

The RISC vs CISC debate is over because there is no longer anything to debate.

As Jon Stokes says in his article RISC vs CISC: the Post-RISC Era, "by now, it should be apparent that the acronyms 'RISC' and 'CISC' belie the fact that both design philosophies deal with much more than just the simplicity or complexity of an instruction set... In light of what we now know about the historical development of RISC and CISC, and the problems that each approach tried to solve, it should now be apparent that both terms are equally nonsensical... Whatever 'RISC vs. CISC' debate that once went on has long been over, and what must now follow is a more nuanced and far more interesting discussion that takes each platform–hardware and software, ISA and implementation–on its own merits.".

Alternatives

While RISC and CISC have been the most popular Instruction Set Architectures over the last 40 years, they aren't the only ones out there.

For example, Explicitly Parallel Instruction Computing (EPIC) was used in Intel's Itanium processor launched in 2001 (Hewlett-Packard, 2001). According to Hewlett-Packard, the idea of EPIC was to allow processors to execute instructions

on the compiler rather than on the circuitry itself. However, EPIC never took off and the Itanium processors were discontinued in 2021 (Intel, 2019).

Another alternative to RISC and CISC was the Minimal instruction Set Computer (MISC) which attempted to use even fewer instructions than RISC chips (Ting and Moore, 1995). MISC has rarely been used in mainstream computing.

The final, and most radical, alternative to RISC and CISC architectures is the Ultimate Reduced Instruction set computer (URISC) which only has one instruction. This architecture is mainly used as a teaching tool for novice students (Mavaddat and Parhami, 1988).

The Future

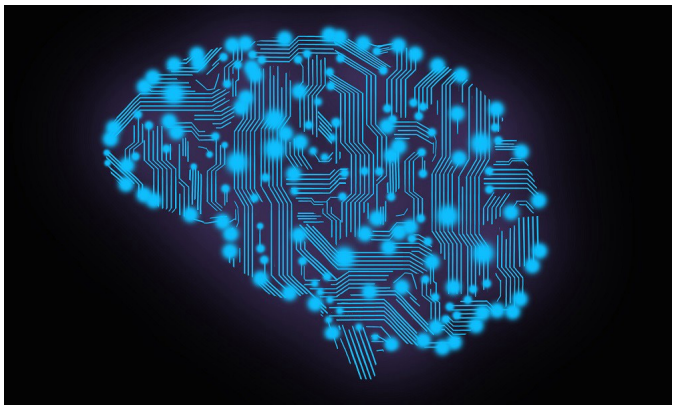
In 2010, the first open-source RISC processor was created by the University of California, Berkely called RISC-V (pronounced "RISC five"). While RISC-V has been primarily used by small developers, it is now trying to compete with larger processor manufacturers like Intel. In 2021, RISC-V announced the world's first full-stack open source processors called the Xuantie Series in partnership with Alibaba (RISC-V, 2021). According to RISC-V these processors "will promote the maturity of RISC-V architecture and help accelerate the integration and development of RISC-V software and hardware technologies" (2021).

Another interesting development in Instruction Set Architecture (ISA) is the idea of the Zero Instruction Set Computer or ZISC. These computers seek to do away with instruction sets completely and instead attempt to use neural networks to perform tasks (Lambinet, 2015). According to Lambinet, the first ZISC chip (the ZISC36) was launched in 1993 when a small research team approached IBM. Since then, major developments in ZISC technology have taken place and companies like Intel and Qualcomm have gotten involved (Lambinet, 2015). According to Lambinet, ZISC chips may allow us to build smart pet doors, have EEG machines that can recognize the warning signs of an irregular heartbeat and may even allow us to download our consciousness onto a computer so that we can live forever (Lambinet, 2015).

RISC-V®

RISC-V: The Free and Open RISC Instruction Set Architecture

The official RISC-V logo. Credit: RISC-V.



The future of computing may simulate the brain using neural networks. Credit: Startup Health.

Discussion

This paper was a very valuable experience for me.

Through writing and researching for it, I was able to strengthen my understanding of the ISA concepts we learned in class. I was also able to learn how ISA applies to modern-day computers and even how it may become obsolete in the future. We learned a lot about the technical side of a computer's instruction set in class and this research paper allowed me to strengthen that understanding by examining computer architecture from a broader view.

While RISC vs CISC is now an obsolete debate, understanding a computer's instruction set is still very important for omputing. As mentioned earlier, a computer's instruction set allows it to run programs and if a computer can't run programs, it becomes useless. Understanding a processor's instruction set can also help developers write more efficient code based on the commands the instruction set can perform and is also useful for debugging.

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